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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,846	12/04/2003	Chien-An Yu	10113381	7437

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EXAMINER	
DAHIMENE, MAHMOUD	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,846	YU, CHIEN-AN	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 recites the limitation "the hard mask structure" as the preamble. There is insufficient antecedent basis for this limitation in the claim, improper preamble.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,2,11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over anonymous research disclosure RD 441003 (Research Disclosure Journal, ISSN 0374-4353) in view of Yoo et al. (US 6033969).

Applicant claims a method for rounding the top corner of a trench, comprising the steps of: forming a masking layer overlying a substrate; patterning the masking layer to form at least one opening therein to expose the substrate and form a recess region in the substrate; oxidizing the recess region to form a first oxide layer thereon to round the top corner of the recess region; successively etching the first oxide layer and the substrate under the opening to form the trench in the substrate; and conformably forming a second oxide layer on the surface of the trench.

RD 441003 discloses a method for forming rounded shallow-trench corners for high voltage flash cell operation by means of a dual trench oxidation process the method consists of the following steps (page 1 of disclosure):

- after growing a pad oxide layer and depositing a layer of silicon nitride on a semiconductor substrate, nitride is patterned for active-region definition and a shallow trench is etched into the substrate which reads on "forming a masking layer overlying a substrate; patterning the masking layer to form at least one opening therein to expose the substrate and form a recess region in the substrate".

- after cleaning the wafer in hydrofluoric acid and deionized water, a layer of oxide is grown on the wafer, the oxide layer is less or equal to twice size of the pad oxide which reads on "oxidizing the recess region to form a first oxide layer thereon to round the top corner of the recess region";

- a second chemical clean is performed on the wafer, etching away almost the entire first oxide layer which reads on "successively etching the first oxide layer".

- another oxidation is performed on the wafer to round the sharp shallow-trench corner which reads on "conformably forming a second oxide layer on the surface of the trench".

A difference is noted between applicants claim 1 and the research disclosure RD 441003, in applicants claim 1 the trench is etched after removal of the first oxide whereas in RD 441003 the trench is etched prior to the first oxide growth.

Yoo discloses a method for forming a shallow trench isolation that has rounded and protected corners by first forming a bird's beak field oxide layer(50) prior to

the trench-forming step such that a rounded and protected top corner (52) and a rounded bottom corner of the trench(62) can be formed. The top corner of the trench opening is protected by the beak portion of the bird's beak against etching in a subsequent oxide dip process before gate formation. As in the applicants claim 1, Yoo opens the pad oxide and nitride mask to expose the silicon substrate (column 2, line 53), the forming an oxide layer, the etching the oxide (column 2, line 59), and then etching the silicon substrate (column 2, line 61).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of the reference RD 441003 to include the teachings of Yoo because a double oxidation is desirable for rounding top corner of trenches, and particularly, growing the first oxide before etching the trench is desirable because, as disclosed by Yoo, this method has the added benefit of allowing for rounded and protected corners such that dislocation does not occur at the bottom corner of the trench (column 2, line 17).One of ordinary skill in the art would have been motivated to modify the process of the reference RD 441003 to grow the first oxide prior to the silicon trench etch because in addition to obtaining rounded top corners, the modified method allows for rounded bottom corners as well reducing dislocations. The corner rounding effect is controlled by the first oxide thickness, higher oxide thickness yields larger rounding radius for both top and bottom corners.

As to claim 11, the reference of RD 441003 discloses another oxidation is performed (step 4 of the process, page 1), here, it is understood the oxidation has to be thermal oxidation. One of ordinary skill in the art would differentiate between performing

oxidation usually meaning growing a thermal oxide as opposite to oxide deposition which is usually performed by CVD or other means.

As to claim 12, the oxide thickness disclosed by Yoo is about 100-200 Angstroms (Column 4, line 21) which includes the range claimed by the applicant.

Claims 3, 4,13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over reference RD 441003 in view of Yoo et al. (US 6033969), and further, in view of Akatsu et al. (US 20050026382).

It is noted that the modified method of RD 441003 as described above does not include a BSG layer as a hard mask on top of the said masking layer as claimed by the applicant (claim 3, page 10, line 3).

Akatsu discloses a method for improved trench processing where BSG (240) is used as a hard mask to pattern the said masking layer (page 3, paragraph 37, and figure 2). Process steps associated with the deposition and etch of the BSG layer are also described.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of reference RD 441003 to include an additional BSG layer because reference of Akatsu illustrates a hard mask is desirable because it prevents modification of the lithographic critical dimensions during the opening of the said masking layer as photoresist could be eroded or affected by the mask layer opening etch step. One of ordinary skill in the art would have been

motivated to include an additional inorganic hard mask layer in order to obtain a better control of the critical dimensions as defined by the lithography in the photoresist mask.

As to claim13, the method of reference RD 441003 as modified by Akatsu results in forming a shallow trench isolation structure as described in applicant's claim 13.

As to claims 4 and 14, Akatsu discloses a method where etching is performed to pull back the pad stack (230) (page 4, paragraph 41) which reads-on "removing portions of the opening in the sidewalls", the removal of the BSG layer (240) is also described (page 5, paragraph 52).

4. Claims 7,8,9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over reference RD 441003 in view of Yoo et al. (US 6033969) and further in view of Ajmera et al. (US 20020072196).

The method of reference RD 441003 as described above discloses a first oxidation layer.

A difference is noted between the applicant's claim and the reference of RD 441003 which fails to specifically disclose a rapid thermal oxidation method for layer the said first oxide layer.

Ajmera discloses a shallow trench isolation method where the trench sidewalls ((16), figure 5) are oxidized using a rapid thermal oxidation method performed at

1150°C for 30-200 seconds yielding an oxide thickness of 20-300 Angstroms (page 4, paragraph 32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of reference of RD 441003 to substitute an RTO step for a conventional oxidation furnace step, as RTP is becoming increasingly more available in semiconductor manufacturing facilities. One of ordinary skill in the art would have been motivated to use an RTO step to use equipment already available, thereby lowering the cost of the manufactured chips.

5. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over anonymous research disclosure RD 441003 (Research Disclosure Journal, ISSN 0374-4353) in view of Yoo et al. (US 6033969), in view of Akatsu et al. (US 20050026382), and further in view of Fuller et al. (US 6174787).

The method of reference RD 441003 modified by Akatsu, as described above is silent about the specific method for the mask layer pullback as described by applicant's claims 5 and 15.

Fuller discloses a silicon corner rounding method for shallow trench isolation where the masking layer (oxide and nitride) (104) is recessed or pulled-back using a HF/EG solution (column 4, lines 15-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of RD 441003 and Akatsu to include the teachings of Fuller in order to obtain an isotropic etch for pulling back the

mask layer. One of ordinary skill in the art would have been motivated to use HF or EG to pull back the masking layer because, as indicated by Fuller, this method in conventionally used in semiconductor processing.

Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over anonymous research disclosure RD 441003 (Research Disclosure Journal, ISSN 0374-4353) in view of Yoo et al. (US 6033969), in view of Akatsu et al. (US 20050026382), and further in view of Kim (KR 2003039385).

The method of reference RD 441003 modified by Akatsu, as described above is silent about the specific depth of the recess region as described by applicant's claims 6 and 16.

Kim describes a method for forming trench of semiconductor device to prevent damage of trench corner by forming rounded trench corner using a two step etch process where the substrate (10) is etched to the depth of 200-300 Agstroms by the first etch process (see sbstact).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of RD 441003 and Akatsu to include the teachings of Kim to remove 100 to 300 Angstroms from the substrate because removal of the top substrate surface allows reduction of potential damage from top substrate surface (micro-scratches) and allows formation of rounded corner during first oxidation. The difference in ranges between applicant's claims 6 and 16 and the reference of Kim is within the etch depth control range. One of ordinary skill in the art

would have been motivated to remove a thin layer of the substrate surface to improve damage performance of the resulting device.

6. Claims 17,18,19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over research disclosure RD 441003 (Research Disclosure Journal, ISSN 0374-4353) in view of Yoo et al. (US 6033969), in view of Akatsu et al. (US 20050026382) and further in view of Ajmera et al. (US 20020072196).

The method of RD 441003 modified by Akatsu does not specify detailed conditions for the recess oxidation process as described by applicant's claims 17-20.

Ajmera discloses a shallow trench isolation method where the trench sidewalls ((16), figure 5) are oxidized using a rapid thermal oxidation method performed at 1150°C for 30-200 seconds yielding an oxide thickness of 20-300 Angstroms (page 4, paragraph 32) and.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of RD 441003 and Akatsu to substitute an RTO step for a conventional oxidation furnace step, as RTP is becoming increasingly more available in semiconductor manufacturing facilities. One of ordinary skill in the art would have been motivated to use an RTO step to use equipment already available, thereby lowering the cost of the manufactured chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571)

272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Muhmood Dahimene

MD

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER